

FREQUENCY DOMAIN EQUALIZER FOR WIRELESS COMMUNICATIONS SYSTEM

BACKGROUND OF THE INVENTION

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Field of Invention

[0001] The present invention relates to wireless communications and is particularly applicable, but not limited to, devices and modules for correcting errors introduced to a wireless signal after its transmission.

Description of the Related Prior Art

[0002] The ongoing revolution in communications technology has led to advances in wireless or radio technology. Wireless technology is currently being used in such disparate fields as wireless computer networks and wireless telephony. One technology which has been favoured for these applications is called Orthogonal Frequency Division Multiplexing (OFDM). As will be appreciated by those in the art, Frequency Division Multiplexing (FDM) involves using different frequencies to carry different signals, but this normally also involves providing a large “guard band” between the different frequencies. With OFDM, intersymbol interference (ISI) or interference between the different signals due to the closeness of their carrier frequencies is reduced as a special set of signals is used to build the transmitted composite signal. As a result of

this feature, smaller guard bands are required and a more efficient use of bandwidth/resources can be achieved.

[0003] While OFDM has been successful in increasing the amount of data which is now transmitted over wireless links, much like any wireless technology, it is still subject to the limitations of the medium. Since signals are transmitted by radio waves, these signals may still suffer from not only distortions introduced by the act of transmission itself, but also from possible errors introduced by signal processing. Time-varying channel distortions, residual carrier frequency offsets, and residual sampling frequency offsets can distort and corrupt each OFDM signal.

[0004] A time domain OFDM signal consists of frames of samples corresponding to the data symbols (data frames), each frame preceded by a cyclic prefix of known length (a guard frame). At the input of the Fast Fourier Transform (FFT), the time domain signal is framed in accordance with the positioning of the data and guard frames in the signal.

[0005] Referring to Figure 1, in a typical operating environment, transmitted radio waves comprise of a number of subcarrier signals are reflected off various surfaces. As a result, the signal received at a base station may come from different directions (depending on reflections) with different strength (depending on attenuations), and the receiver sees only the combinations of all these reflections. This phenomenon is called multipath. The main problem of multipath is that it creates delay spread. Depending on the number of reflections and the propagation speed in different signals, all these signals generally do not arrive exactly at the same time at the receiver. The main technique to overcome delay spread is equalization. An equalizer attempts to invert or correct the effects of transmission distortion and signal processing errors. More specifically, an equalizer is a digital circuit that attempts to estimate the distortion due to the signal propagation through different paths, which effects each component's relative timings, phase and strength. The equalizer estimates the distortion and removes the distortion. A digital equalizer is often implemented as a time-domain digital finite response filter (FIR)

adaptive taps, or as a frequency domain filter with an adaptive tap for each frequency point of concern.

[0006] More specifically, under the IEEE 802.11a standard relating to low power wireless devices, a data symbol bearing 64 samples is preceded by a 16 sample cyclic prefix, yielding a total of 80 samples. A 64-point FFT is applied to a frame of 64 samples (an FFT frame). To reduce inter-symbol-interference, an FFT framing offset with respect to the start of the data frame is applied. With an FFT framing offset of 5 samples, the FFT frame of length 64 would then start at the 12th sample of the guard frame and end at the 59th sample of the data frame.

[0007] An FFT offset is, in fact, a negative delay of the FFT frames with respect to the data frames. When applied during channel estimation, the offset therefore introduces a phase rotation corresponding to that delay, a rotation which is in addition to any other phase and gain distortion already present in the channel without the delay. It is the sum of these distortions which an equalizer attempts to correct. The channel distortions include distortion due to multipath, as well as distortions due to the analogue and digital signal processing in the transmitter and receiver.

[0008] The phase rotation due to the delay causes a linear distortion on the real and imaginary components of each subcarrier's channel estimate, which makes channel estimate smoothing difficult if not impossible.

[0009] Equalizers for wireless communications systems are known in the art. For example, US 6,327,302 entitled "Systems and Methods of Digital Wireless Communication Using Equalization" issued December 4, 2001 and assigned to Ericsson Inc., describes a method and apparatus to accomplish fast adaptive equalization of a wireless communication channel utilizing time varying adaptive filter coefficients and convergence parameters. Although the technique described in this patent for a time domain equalizer works adequately, it is focused solely on overcoming channel

distortions and does not address possible errors introduced by residual carrier frequency offsets, and residual sampling frequency offsets.

[00010] Another prior art equalizer is described in US 6,389,062 entitled Adaptive Frequency Domain Equalizer Circuits, Systems and Methods For Discrete Multitone Based Digital Subscriber Line” issued May 14, 2002 and assigned to Texas Instruments Inc.. This patent illustrates a channel equalization system using a combined frequency domain equalizer for use in a digital subscriber line (DSL) modem. The system adjusts for amplitude and phase distortions in a received signal but does not address possible errors introduced by residual carrier frequency offsets, and residual sampling frequency offsets. It is also not adapted for a wireless network utilizing OFDM.

[00011] Based on the above, there is therefore a need for a device which overcomes channel distortions and compensates for possible errors introduced by residual carrier frequency offsets and residual sampling frequency offsets. Ideally, such a device can compensate for all three deleterious effects, while being self-contained and monolithic.

SUMMARY OF THE INVENTION

[00012] The present invention provides a frequency domain equalizer which compensates for undesirable effects on received radio signals introduced by either signal processing or by the transmission medium. In operation, the equalizer multiplies the complex received signal after transformation into the frequency domain with a complex corrective signal that compensates for these effects. A time-varying tap corrective signal corrects for time-varying channel effects (i.e. channel distortions), a timing tracking signal corrects for sampling frequency offset errors, and a phase tracking signal corrects for carrier frequency offset errors. The tap corrective signal is generated by calculating an initial tap value and applying a sign least mean squares (LMS) process or algorithm to the received signal while both the phase tracking signal and the timing tracking signal are

derived from the pilot tones of each OFDM data symbol. Separate phase tracking and timing tracking circuits produce the phase tracking and timing tracking corrective signals.

[00013] In accordance with one aspect of the invention, there is provided a frequency domain equalization system to compensate for wireless communication time-varying channel effects, residual carrier frequency offset and sampling frequency offset arising in a received complex signal comprising: an equalizer tap calculation circuit cooperating with an equalizer tap tracking circuit for correcting the time-varying channel effects; a phase tracking circuit for correcting the residual carrier frequency offset; and a timing tracking circuit for correcting the sampling frequency offset, wherein the received complex signal is inputted from a Fast Fourier Transform (FFT) circuit and a corrected complex signal is outputted to a soft decision mapper; and wherein a corrective tap signal is produced in the equalizer tap calculation circuit for use in correcting the complex signal; and wherein four pilot signals are generated for use in the phase and timing tracking circuits.

[00014] In accordance with another aspect of the invention there is provided in a wireless communications system, a method of correcting a received complex signal comprising: estimating a channel response from long sequence training symbols FFT 1 and FFT 2 contained in a received data packet preamble; processing pilot tones in successive data symbols associated with the FFT 1 and FFT 2 long sequence training symbols to evaluate carrier frequency offset and sampling frequency offset; compensating for any of the carrier frequency or sampling frequency offset in said next received data packet; tracking channel distortion during subsequent reception of data packets; and modifying the channel response to compensate for any detected distortion.

[00015] The advantage of the present invention is now readily apparent. An equalizer with integrated timing recovery and phase tracking is provided which operates in the frequency domain.

BRIEF DESCRIPTION OF THE RELATED PRIOR ART

[00016] A better understanding of the invention will be obtained by considering the detailed description below, with reference to the following drawings in which:

Figure 1 depicts multipath and delay in a wireless system;

Figure 2 depicts a block diagram of a digital receiver in accordance with the present invention;

Figure 3 depicts a block diagram of a digital demodulator integral to the digital receiver of Figure 2;

Figure 4 depicts a block diagram of a digital demodulator back end integral to the digital demodulator of Figure 3;

Figure 5 depicts a timing overview of the equalization process integral to the present invention;

Figure 6 depicts the equalizer tap calculation (channel estimation) circuit;

Figure 7 depicts the equalizer tap tracking circuit;

Figure 8(a) depicts the phase tracking circuit;

Figure 8(b) depicts the phase predictor circuit integral to the phase tracking circuit of Figure 8(a); and

Figure 9 depicts the timing tracking circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[00017] Referring to Figure 2, there is depicted a digital receiver 2 in which the present invention is housed. The preferred digital receiver 2 may be, for example, the ICE5350 Digital Receiver offered by IceFyre Semiconductor Inc. which performs all the physical layer functions defined in the IEEE 802.11a standard, but the invention is not meant to be limited to this receiver. The digital receiver 2 is located between the RF Receiver Front End 4 and the Physical Medium Access Control (PHY/MAC) 6. The RF Receiver Front End connects to antennae A and B. As shown in the drawing, the two main blocks within the digital receiver 2 are the digital demodulator 8 and the baseband decoder 10. The digital demodulator 82 recovers the baseband signal by removing carrier offsets, timing offsets, compensating for the channel impairments and demapping the digitally modulated signal. This block is located between the analog-to-digital interface (not shown) and the baseband interface (not shown). The baseband decoder 10 de-interleaves the baseband signal, provides error correction through the soft-decision Viterbi algorithm and unscrambles the corrected bit stream to be passed through the PHY/MAC 6. This block is located between the baseband interface (not shown) and the PHY/MAC interface (not shown).

[00018] Figure 3 depicts the digital demodulator 8 of Figure 1. As shown in the diagram, the analog to digital interface is located at block ADCs/ DACs 12. The baseband interface can also be seen in the figure at the soft decision demapper 14. It can also be seen in the figure that the digital demodulator 8 is distinctly divided into two parts by the Fast Fourier Transform (FFT) circuit 16. To the left is the digital demodulator front-end (DFE) 18, while to the right is the digital demodulator back-end (DBE) 20. The invention of the present invention is provided in the digital demodulator back-end 20.

[00019] Referring to Figure 4, an overview of the DBE is depicted. The DBE performs all digital signal processing (DSP) functions from the FFT circuit 16 output to the soft decision demapper 14 input. As will be more fully described below, in particular, the DBE functions as an equalizer (EQ) (depicted generally at 22) with integrated timing

and phase tracking circuitry (depicted at 24 and 26 respectively). As can be seen in the Figure the phase tracking circuit 26 is nested with the timing tracking circuit 24. All of this functionality is accomplished completely in the frequency domain i.e. after the FFT circuit 16. This is advantageous as the control signals are more easily derived from the frequency domain, where the pilot signals are readily available to reveal phase and timing error i.e. they are a product of the FFT circuit 16. Applying the correction after the FFT circuit 16 also serves to avoid the latency of the FFT circuit 16. As shown in the drawing, the equalizer also includes equalizer tap calculation circuitry 28 and equalizer tap tracking circuitry 30.

[00020] In general, the equalizer compensates each of 52 complex subcarriers of each OFDM symbol for time-varying channel effects, residual carrier frequency offset and residual sampling frequency offset. It accomplishes these functions by estimating an initial channel response from the complex data received in two symbols transmitted in the long sequence training preamble of a data packet. It then processes four pilot tones in each successive data symbol to evaluate carrier frequency offset and sampling frequency offset. Any detected offsets result in the next received symbol being compensated for the above effects. During data packet reception the equalizer tracks changing channel distortion and modifies the calculated taps (discussed below) to minimize the error for each subcarrier received. The 52 complex subcarriers are received from the FFT circuit 16 and after equalization presents the equalized subcarriers to the soft decision demapper 18 in time-division multiplexed even and odd, in-phase and quadrature subcarrier data buses.

[00021] Referring to Figure 5, a timing overview of the equalizer of the present invention is provided. The FFT load signals repeat every 80 clock periods. For a 20 Mhz clock, this time represents the symbol period of the received OFDM data. The first symbol that is processed is FFT 1 of the long sequence training symbol, followed by FFT 2 of the long sequence training symbol. The complex subcarriers of these two symbols are averaged on a per subcarrier basis, then presented to the equalizer tap calculation circuit 28 within the equalizer for initial channel estimation and tap initialization. Each

subcarrier has one associated complex tap that, once initialized, is used to correct for static and time-varying channel effects. The tap corrective signal is generated by calculating an initial tap value and applying a least mean squares (LMS) process or algorithm to the received subcarriers. The taps are used to correct the FFT subcarrier data starting with the SIGNAL symbol. Within the timing-tracking circuit 24, the timing-tracking calculations are initialized at the beginning of each packet. The 52 complex timing-tracking offset correction values are preset based on the FFT framing offset, and hence the offset is transparent to the equalizer tap calculation circuit. Within the phase tracking circuit 26, the phase-tracking calculation is initialized at packet start by initializing a complex register value. During the SIGNAL symbol, four pilot tone subcarriers are extracted and reordered into subcarrier order. A phase tracking rotor is calculated from these four pilot tone subcarriers and applied to the next data symbol. The timing-tracking calculations also calculate new timing-tracking offset correction values (in the form of a time tracking rotor) from the same four pilot tone subcarriers and apply these values to the next data symbol on a subcarrier basis.

[00022] With respect to the equalizer tap calculation, the amplitude and phase distortion as seen by the equalizer tap calculation circuit 28 in each data and pilot subcarrier translate to equalizer tap values. Tap values are the complex inverse of the channel estimate. The complex inverse returns inverse amplitude and a conjugate angle. Referring to Figure 6, greater detail of the equalizer tap calculation circuit 28 is given. Channel estimation is performed by comparing (at 34) the received amplitude and phase of the transmitted long symbol 36 with a reference amplitude and phase which is the local replica of the long symbol at the receiver. Comparison is performed by multiplying (demodulating) (at 38) the received value in each subcarrier with the local long symbol. Averaging (at 40) over FFT 1 and FFT 2 precedes the multiplication (at 38), in order to enhance the estimate under zero-mean noise conditions.

[00023] Further enhancement of the estimate is obtained through spectral smoothing (at 42). Since the degree of correlation of noise between subcarriers is well below the degree of correlation of the channel phase and magnitude between subcarriers,

an averaging across subcarriers provides additional enhancement. Spectral smoothing is performed through three-tap or five-tap complex moving average across the data and pilot subcarriers, with special consideration of the band edges. Under some harsh conditions, whereby deep nulls cause severe linear distortion, smoothing may, to some degree, have an adverse effect. Under such circumstances, no smoothing or smoothing with only three taps is preferable. In contrast, under flat channel conditions, smoothing delivers significant improvement and five taps are preferred. The smoothing circuit can be programmed to allow for such selections. Any non-zero symbol delay (i.e. FFT framing offset) after symbol framing at the input to the FFT circuit 16 will emerge as a phase rotation of the estimated spectrum. A phase rotation manifests itself as a cosine and sine shaped distortion, and a spectrum that is otherwise sufficiently fit for smoothing, becomes unfit. Since a significant share of the non-zero symbol delay is known and intentional, appropriate timing correction is applied to the input to the channel estimator. This correction is performed by the timing recovery circuit, when it is preset and held during the long symbol.

[00024] Referring to Figure 7, the equalizer tap tracking circuit 30 is more fully depicted. The function of the equalizer tap tracker 30 is to refine tap values, track residual phase and timing error, and track channel variations. Tap updating is performed with a running time average of a slicer error (shown at 44). The tap update allows the equalizer to adjust the taps to an expanding and diminishing constellation, as well as a rotating constellation. It compensates for phase lag and amplitude distortions by the timing and phase tracking circuits to be discussed later. It also refines (at 46) the initial tap values obtained from channel estimation, a typically imperfect estimation due to noise. Tap tracking can be turned on and off as required. The signal that drives the tap values is provided by the slicer 48. At each symbol and for each data subcarrier, the slicer 48 returns the complex difference (error) between the constellation value at its input and the nearest odd integer constellation point corresponding to the applicable constellation size. This error is normalized (at 50) based on the constellation size prior to being used for updating (at 52) the tap value. Time averaging is essential to reduce tap jitter, and such averaging is accomplished through scaling of the normalized slicer 48.

[00025] Figure 8(a) depicts in greater detail the phase tracking circuit 26, while Figure 8(b) depicts a phase predictor circuit integral to the phase tracking circuit 26. The purpose of the phase tracking circuit 26 is to correct for residual carrier frequency offset, after adjustments by the digital front-end numerically controlled oscillator (DFE-NCO) (shown as 32 in Figure 4). Residual offsets are a result of inaccurate offset estimations during the short symbol and the long symbol in the preamble. The DFE-NCO corrects sufficiently for the FFT, yet additional correction after the FFT is needed, especially for packets of intermediate to maximum length, and packets with higher density constellations. The phase error causes the constellations to rotate up to a few degrees per symbol. Although the equalizer would be capable of tracking this residual rotation, phase tracking using four pilots is more robust under noisy conditions. The equalizer adaptation is thus capable of operating with a time constant too slow to track the phase error. The circuit tracks the phase across the four equalized pilots 54 using time averaging (at 56) and averaging across the pilots as well as phase prediction (at 58). Importantly, the pilot equalizer taps do not adapt, and hence the rotation is entirely visible to the phase tracking circuit. For correction, a rotor 60 which represents the reverse drift is applied to the pilot and data subcarriers in a feed forward manner.

[00026] Referring to Figure 9, the timing tracking circuit 24 is depicted. The function of this circuit is to track timing error due to sampling frequency offset. The received signal is sampled at the ADC 12 (Figure 3) with a clock derived from the device clock (not shown) of the digital receiver 2 (Figure 2). A difference in clock frequency between the clock used for transmission and the clock used for sampling in the receiver, manifests itself as a stretching or shrinking of the received baseband spectrum. This stretch or shrinkage causes a subcarrier frequency offset, which increases with the distance of the subcarrier from direct current. Such a timing offset causes a phase rotation similar to that of a carrier frequency offset, but the speed of the offset varies per subcarrier. This timing error causes the constellations to rotate up to 0.5 degrees per symbol in the outer most carrier.

[00027] Although the equalizer would be capable of tracking this residual rotation, timing tracking using four pilots is more robust under noisy conditions. The equalizer adaptation is thus capable of operating with a time constant too slow to track the timing error. The circuit tracks the phase across the four equalized pilots using time averaging (at 64) across the pilots. Importantly, the pilot equalizer taps do not adapt, and hence the rotation is entirely visible to the phase tracking circuit 26. For correction, a main rotor phase (at 66) which represents the reverse timing drift, is used as the basis for calculating an individual rotor phase for each subcarrier. The individual rotors are applied to the pilot and data subscribers in a feed back manner. The timing tracking circuit is also used to undo the phase rotation due to an intentional FFT framing offset into the guard interval. Correction of the phase before the equalizer tap calculation is required for the spectral smoothing circuit. The initial phase of the main rotor is read from a register, and it is not updated by the circuit during the long symbol. Thereafter, the timing tracking circuit will update the rotor.

[00028] As will be appreciated by those in the art, within the frequency domain, a complex FFT output can be represented by $X(K,n)$ where time $n=1..N$ OFDM FFT frames (OFDM symbols), including training symbols, and where K is the subcarrier index. More specifically, in accordance with IEEE 802.11a, active sub-carrier indices are frequency indices $K=-26..0..26$ (52 sub-carriers), among which pilot sub-carrier indices are $K_P=-14,-7,7,14$ (i.e. 4 pilots). Data sub-carrier indices are $K_D=-26..-15, -13..-8, -6..-1, 1..6, 8..13, 15..26$ (i.e. 48 data carriers). The training symbols consist of two FFT frames with fixed and known binary phase shift keying (BPSK) modulation in each subcarrier. Transmission of data symbols follows the transmission of training symbols.

[00029] The processing steps for channel estimation, adaptive equalization, and phase and timing tracking are will now be now explained in more detail with reference to Figures 4 and 6 to 9, where the circled numbers represent the portion of the depicted circuit where the steps defined below are performed:

(a) Perform the following during reception of the training symbols:

101. Reset a symbol counter to $n=1$;
102. For each subcarrier, initialize a complex timing correction $T(K,n)$ based on the FFT framing offset: set $T(K,1)=\exp(-j 2 \pi K d / M)$ whereby d is the FFT framing offset (samples, $d>0$) and M is the size of the FFT frame (samples). Typically M corresponds to the size of the FFT;
103. Reset a phase correction $P(n)$: set $P(1)=0$;
104. For each subcarrier, reset a channel estimation accumulator $A(K,n)$: set $A(K,1)=0$;
105. For each subcarrier, apply the timing correction to the output of the FFT $X(K,n)$: $X'(K,n)=T(K,n) X(K,n)$;
106. For each sub-carrier, accumulate the received training symbol: $A(K,n)=A(K,n)+X'(K,n)$;
107. Maintain (freeze) the phase correction: $P(n+1)=P(n)$;
108. Maintain (freeze) the timing correction: $T(K,n+1)=T(K,n)$;
109. Increment the symbol counter: set $n = n+1$;
110. Repeat steps 105 to 109 for the duration of all training symbols. In the above the transmitted training symbols are assumed to be constant over time;
111. For each subcarrier, calculate a channel estimate $C(K) = A(K,n)/L(k)/(n-1)$ whereby $L(K)$ is the transmitted training symbol;
112. Optionally, smooth the channel estimate to obtain a spectrally smoothed channel estimate $C'(K)$ for each subcarrier;
113. For each subcarrier calculate initial equalizer taps $W(K,n)=1/C'(K)$.

[00032] In IEEE 802.11a, the training symbols consist of two FFT frames in a so-called Long Symbol. Therefore, we proceed with $n=3$. Also, the training symbol $L(k)$ is BPSK (values of +1 and -1) and therefore the division by $L(K)$ in step 111 can be replaced by a multiplication with $L(K)$, arriving at $C(K) = A(K,n)L(k)/2$.

(b) Perform the following processing related to the equalizer during reception of the data symbols:

114. For each subcarrier, apply the timing correction to the output of the FFT
 $X'(K,n) = T(K,n) X(K,n)$;
115. Demodulate the pilot carriers with their known modulation $M(K_P,n)$,
 (again assuming that the modulation is BPSK, multiplication suffices)
 and apply the equaliser: $X''(K_P,n) = X'(K_P,n)M(K_P,n)W(K_P,n)$;
116. For each pilot carrier apply the phase correction: $Z(K_P,n) = X''(K_P,n)P(n)$;
117. For each data carrier, apply the phase correction: $Y(K_D,n) = X'(K_D,n)P(n)$;
118. For each data carrier, apply the equalizer: $Z(K_D,n) = Y(K_D,n)W(K_D,n)$;
119. For each data carrier, apply a constellation denormalisation factor F :
 $Z'(K_D,n) = F Z(K_D,n)$;
120. For each data carrier, perform a hard decision based on the equalizer
 output $Z(K_D,n)$. This is accomplished by slicing the equalizer output
 based on the constellation at hand to obtaining the decision result
 $D(K_D,n)$. For instance, for a 16-Quadrature Amplitude Modulation
 (QAM - a combination of amplitude modulation and phase shift keying)
 sub-carrier that is normalised to an average power level equaling one,
 the equalizer output is denormalised with a constellation
 denormalisation factor, which for 16-QAM equals $\sqrt{10}$, and slicing is
 performed based on real and imaginary decision boundaries at 0 and
 ± 2 while selecting the nearest ideal 16-QAM constellation point with
 ideal real component values of ± 1 and ± 3 , and with ideal imaginary
 component values of ± 1 and ± 3 . The 16 possible values for $D(K_D,n)$
 are thus $\pm 1 \pm 1j$, $\pm 1 \pm 3j$, $\pm 3 \pm 3j$ and $\pm 3 \pm 1j$;
121. For each data carrier, calculate a complex slicer error $E(K_D,n)$ whereby
 $E(K_D,n) = Z(K_D,n) - D(K_D,n)$;
122. For each data carrier, apply a constellation normalisation factor $1/F$:
 $E'(K_D,n) = (1/F) E(K_D,n)$;

123. For each data carrier, calculate an equalizer tap update $w(K_D, n)$:
 $w(K_D, n) = E'(K_D, n) \text{conj}(\text{sign}(Y(K_D, n)))$ in which
 E' is an update parameter, the value of which is a tradeoff between speed and tap jitter. A suitable setting is
 $\text{conj}(x)$ returns the complex conjugate of x , and
 $\text{sign}(x)$ returns the complex sign of x , being $\pm 1 \pm j$;
124. Update the equalizer taps for the data carriers:
 $W(K_D, n+1) = W(K_D, n) + w(K_D, n)$

[00032] As an alternative to the two multiplications for denormalization by F and normalization by $1/F$, it is possible to incorporate factor F in the equalizer taps. This is performed when the modulation changes. For instance, after a BPSK symbol and before a subsequent 16-QAM symbol all equalizer taps are multiplied with $\sqrt{10}$. As can be seen in Figure 4, the equalizer tap multiplier is present but the denormalization multiplier is absent. In this arrangement, the denormalization factor is incorporated in the equalizer taps. This is in contrast to Figure 7 where two separate multiplications are performed for normalization and denormalization.

(c) Perform the following processing related to the phase correction during reception of the data symbols:

125. Calculate a common phase rotation by summing over the demodulated and equalised complex pilots: $S(n) = \text{sum}(X''(K_P, n))$ (ie sum for all K_P). For 802.11a this yields $S(n) = S(7, n) + S(14, n) + S(-7, n) + S(-14, n)$;
126. Filter the common phase rotation with a complex Low Pass Filter, e.g. implemented by two Leaky Integrators (LI), one for the real part of $S(n)$ and one for its imaginary part. The LI is a first order Infinite Impulse Response (IIR) with coefficient :
 $S'(n) = S(n) + (1 - \alpha)S'(n-1)$
Initialize the LI with $S'(2) = 0$;

127. Apply a predictor to reduce the impact of the Low Pass Filter delay:
 $S''(n) = 2S'(n) - S'(n-1);$
128. In preparation for the next iteration, update the phase correction to be the complex conjugate of the predictor output: $P(n+1) = \text{conj}(S''(n));$

[00032] The above steps effectively update the phase of a phase correction rotor $\exp(-j\theta)$, whereby phase θ is obtained by averaging the common phase error of the pilots.

(d) Perform the following processing related to the timing correction during reception of the data symbols:

129. For each pilot carrier at the input to the timing tracking circuit, determine the sign of its frequency index and then sum the imaginary parts of the pilots multiplied by the sign of their indices:
 $V(n) = \sum (\text{imag}(Z(K_p, n)) \text{sign}(K_p))$ (i.e. sum for all K_p considering the sign of each value of K_p)

For 802.11a this yields $V(n) = \text{imag}(Z(7, n)) + \text{imag}(Z(14, n)) - \text{imag}(Z(-7, n)) - \text{imag}(Z(-14, n))$

Considering that the feedback timing correction keeps the timing error induced phase of the pilots at this point in the circuit small, the phase can be approximated by the sum of the imaginary component of the pilots. Consider also that, for a given delay, the sign of the phase error for positive frequencies is negated in regards to the sign of the phase error for negative frequencies;

130. Filter the common phase rotation with a Low Pass Filter, e.g. a Leaky Integrator (LI) which is a first order IIR with coefficients α and $1-\alpha$ and apply a gain G to obtain a phase increment $V'(n)$
 $V'(n) = G(V(n) + (1-\alpha)V'(n-1))$

The above arrangement allows each of the filter coefficients and the gain

to be approximated by a power of two, removing the need for a fixed point multiplier in favour of a binary shifter. Suggested values are

131. Accumulate the phase increment to obtain the phase of the timing correction:

$$V''(n) = V''(n-1) + V'(n)$$

Initialize with $V''(3) = 0$;

132. In preparation for the next iteration, convert the phase to an individual conjugate rotor for each subcarrier:

$T(K, n+1) = \exp(-j V''(n) K)$. This step is best performed with a CORDIC circuit;

133. Increment the symbol counter: $n = n+1$; and

134. Repeat steps 114 to 133 for the duration of all data symbols.

[00033] In IEEE 802.11a the Long Symbol is followed first by a BPSK Signal Symbol before the data symbols. Within the context of the above, the Signal Symbol is to be treated as a data symbol.

[00034] The phase correction circuit ensures that the timing correction circuit is presented with demodulated pilots that are substantially void of a common phase error, allowing the extraction of a timing error related phase by summing the imaginary parts of the phasors while considering the sign of their frequency index.

[00035] The timing correction circuit ensures that the phase correction circuit as well as the timing correction circuit itself are presented with demodulated pilots that are substantially void of a timing error related pilot phase error, allowing the approximation of the timing error related pilot phase error by the imaginary component of the pilot phase.

[00036] The present invention may be implemented as a combination of both hardware and software. In particular, the present invention can be implemented as a series of computer readable instructions stored in a microprocessor - a digital signal processor (DSP) ideally suited to the numerically-intensive requirements of equalization as discussed above. The computer readable instructions may be programmed in a procedural programming language (e.g. "C") or an object oriented language (e.g. "C++"). The series of computer instructions embody all or part of the functionality previously described herein. Alternately, the present invention may be implemented entirely in hardware such as an integrated circuit for use in a digital receiver.

[00037] Embodiments of the present invention may also be implemented as a computer program product for use with a computer system. Such implementation may include a series of computer instructions fixed either on a tangible medium, such as a computer readable medium (e.g., a diskette, CD-ROM, ROM, or fixed disk) or transmittable to a computer system, via a modem or other interface device, such as a communications adapter connected to a network over a medium. The medium may be either a tangible medium (e.g., optical or electrical communications lines) or a medium implemented with wireless techniques (e.g., microwave, infrared or other transmission techniques). It is expected that such a computer program product may be distributed as a removable medium with accompanying printed or electronic documentation (e.g., shrink wrapped software), preloaded with a computer system (e.g., on system ROM or fixed disk), or distributed from a server over the network (e.g., the Internet or World Wide Web).

[00038] Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention.

[00039] A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above all of which are intended to fall within the scope of the invention as defined in the claims that follow.